FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The AD9833 has a standard 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 4.

The FSYNC input is a level-triggered input that acts as a frame synchronization and chip enable. Data can be transferred into the device only when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC-to-SCLK falling edge setup time, t_7. After FSYNC goes low, serial data is shifted into the input shift register of the device on the falling edges of SCLK for 16 clock pulses. FSYNC may be taken high after the 16th falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8. Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses and then brought high at the end of the data transfer. In this way, a continuous stream of 16-bit words can be loaded while FSYNC is held low, FSYNC only going high after the 16th SCLK falling edge of the last word loaded.

SCLK can be continuous, or alternatively, it can idle high or low between write operations, but it must be high when FSYNC goes low (t_{11}).

For an example of programming the AD9833, see the AN-1070 Application Note, *Programming the AD9833/AD9834*, at www.analog.com.

POWERING UP THE AD9833

The flowchart in Figure 26. shows the operating routine for the AD9833. When the AD9833 is powered up, the part should be reset. This will reset appropriate internal registers to zero to provide an analog output of midscale. To avoid spurious DAC outputs while the AD9833 is being initialized, the reset bit should be set to 1 until the part is ready to begin generating an output. RESET does not reset the phase, frequency, or control registers. These registers will contain invalid data, and therefore, should be set to a known value by the user. The reset bit should then be set to 0 to begin generating an output. The data will appear on the DAC output eight MCLK cycles after reset is set to 0.

LATENCY

Associated with each asynchronous write operation in the AD9833 is a latency. If a selected frequency/phase register is loaded with a new word, there is a delay of seven to eight MCLK cycles before the analog output will change. (There is an uncertainty of one MCLK cycle, because it depends on the position of the MCLK rising edge when the data is loaded into the destination register.)

CONTROL REGISTER

The AD9833 contains a 16-bit control register that sets up the AD9833 as the user wants to operate it. All control bits, except mode, are sampled on the internal negative edge of MCLK.

Table 6 describes the individual bits of the control register. The different functions and the various output options from the AD9833 are described in more detail in the Frequency and Phase Registers section.

To inform the AD9833 that the contents of the control register will be altered, D15 and D14 must be set to 0 as shown in Table 5.

Table 5. Control Register

D15	D14	D13	D0
0	0	Control Bits	

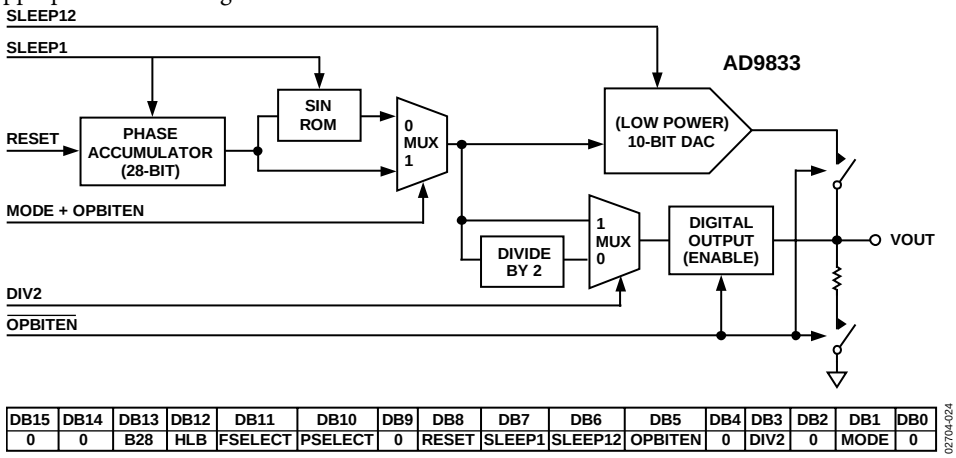

Figure 24. Function of Control Bits

Table 6. Description of Bits in the Control Register

Bit	Name	Function
D13	B28	Two write operations are required to load a complete word into either of the frequency registers. B28 = 1 allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains the 14 LSBs of the frequency word, and the next write contains the 14 MSBs. The first two bits of each 16-bit word define the frequency register to which the word is loaded and should, therefore, be the same for both of the consecutive writes. See Table 8 for the appropriate addresses. The write to the frequency register occurs after both words have been loaded; therefore, the register never holds an intermediate value. An example of a complete 28-bit write is shown in Table 9. When B28 = 0, the 28-bit frequency register operates as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs, and vice versa. To alter the 14 MSBs or the 14 LSBs, a single write is made to the appropriate frequency address. The control bit D12 (HLB) informs the AD9833 whether the bits to be altered are the 14 MSBs or 14 LSBs.
D12	HLB	This control bit allows the user to continuously load the MSBs or LSBs of a frequency register while ignoring the remaining 14 bits. This is useful if the complete 28-bit resolution is not required. HLB is used in conjunction with D13 (B28). This control bit indicates whether the 14 bits being loaded are being transferred to the 14 MSBs or 14 LSBs of the addressed frequency register. D13 (B28) must be set to 0 to be able to change the MSBs and LSBs of a frequency word separately. When D13 (B28) = 1, this control bit is ignored. HLB = 1 allows a write to the 14 MSBs of the addressed frequency register. HLB = 0 allows a write to the 14 LSBs of the addressed frequency register.
D11	FSELECT	The FSELECT bit defines whether the FREQ0 register or the FREQ1 register is used in the phase accumulator.
D10	PSELECT	The PSELECT bit defines whether the PHASE0 register or the PHASE1 register data is added to the output of the phase accumulator.
D9	Reserved	This bit should be set to 0.
D8	Reset	Reset = 1 resets internal registers to 0, which corresponds to an analog output of midscale. Reset = 0 disables reset. This function is explained further in Table 13.
D7	SLEEP1	When SLEEP1 = 1, the internal MCLK clock is disabled, and the DAC output remains at its present value because the NCO is no longer accumulating. When SLEEP1 = 0, MCLK is enabled. This function is explained further in Table 14.
D6	SLEEP12	SLEEP12 = 1 powers down the on-chip DAC. This is useful when the AD9833 is used to output the MSB of the DAC data. SLEEP12 = 0 implies that the DAC is active. This function is explained further in Table 14.
D5	OPBITEN	The function of this bit, in association with D1 (mode), is to control what is output at the VOUT pin. This is explained further in Table 15. When OPBITEN = 1, the output of the DAC is no longer available at the VOUT pin. Instead, the MSB (or MSB/2) of the DAC data is connected to the VOUT pin. This is useful as a coarse clock source. The DIV2 bit controls whether it is the MSB or MSB/2 that is output. When OPBITEN = 0, the DAC is connected to VOUT. The mode bit determines whether it is a sinusoidal or a ramp output that is available.
D4	Reserved	This bit must be set to 0.
D3	DIV2	DIV2 is used in association with D5 (OPBITEN). This is explained further in Table 15. When DIV2 = 1, the MSB of the DAC data is passed directly to the VOUT pin. When DIV2 = 0, the MSB/2 of the DAC data is output at the VOUT pin.
D2	Reserved	This bit must be set to 0.
D1	Mode	This bit is used in association with OPBITEN (D5). The function of this bit is to control what is output at the VOUT pin when the on-chip DAC is connected to VOUT. This bit should be set to 0 if the control bit OPBITEN = 1. This is explained further in Table 15. When mode = 1, the SIN ROM is bypassed, resulting in a triangle output from the DAC. When mode = 0, the SIN ROM is used to convert the phase information into amplitude information, which results in a sinusoidal signal at the output.
D0	Reserved	This bit must be set to 0.

FREQUENCY AND PHASE REGISTERS

The AD9833 contains two frequency registers and two phase registers, which are described in Table 7.

Table 7. Frequency/Phase Registers

Register	Size	Description
FREQ0	28 bits	Frequency Register 0. When the FSELECT bit = 0, this register defines the output frequency as a fraction of the MCLK frequency.
FREQ1	28 bits	Frequency Register 1. When the FSELECT bit = 1, this register defines the output frequency as a fraction of the MCLK frequency.
PHASE0	12 bits	Phase Offset Register 0. When the PSELECT bit = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1	12 bits	Phase Offset Register 1. When the PSELECT bit = 1, the contents of this register are added to the output of the phase accumulator.

The analog output from the AD9833 is

$$f_{MCLK}/2^{28} \times FREQREG$$

where *FREQREG* is the value loaded into the selected frequency register. This signal will be phase shifted by

$$2\pi/4096 \times PHASEREG$$

where *PHASEREG* is the value contained in the selected phase register. Consideration must be given to the relationship of the selected output frequency and the reference clock frequency to avoid unwanted output anomalies.

The flowchart in Figure 28 shows the routine for writing to the frequency and phase registers of the AD9833.

Writing to a Frequency Register

When writing to a frequency register, Bit D15 and Bit D14 give the address of the frequency register.

Table 8. Frequency Register Bits

D15	D14	D13	D0
0	1	MSB 14 FREQ0 REG bits	LSB
1	0	MSB 14 FREQ1 REG bits	LSB

If the user wants to change the entire contents of a frequency register, two consecutive writes to the same address must be performed because the frequency registers are 28 bits wide. The first write contains the 14 LSBs, and the second write contains the 14 MSBs. For this mode of operation, the B28 (D13) control bit should be set to 1. An example of a 28-bit write is shown in Table 9.

Table 9. Writing 00FC00 to FREQ0 REG

SDATA Input	Result of Input Word
0010 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 1, HLB (D12) = X
0100 0000 0000 0000	FREQ0 REG write (D15, D14 = 01), 14 LSBs = 0000
0100 0000 0011 1111	FREQ0 REG write (D15, D14 = 01), 14 MSBs = 003F

In some applications, the user does not need to alter all 28 bits of the frequency register. With coarse tuning, only the 14 MSBs are altered, while with fine tuning, only the 14 LSBs are altered. By setting the B28 (D13) control bit to 0, the 28-bit frequency register operates as two, 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs, and vice versa. Bit HLB (D12) in the control register identifies which 14 bits are being altered. Examples of this are shown in Table 10 and Table 11.

Table 10. Writing 3FFF to the 14 LSBs of FREQ1 REG

SDATA Input	Result of Input Word
0000 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0; HLB (D12) = 0, that is, LSBs
1011 1111 1111 1111	FREQ1 REG write (D15, D14 = 10), 14 LSBs = 3FFF

Table 11. Writing 00FF to the 14 MSBs of FREQ0 REG

SDATA Input	Result of Input Word
0001 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 1, that is, MSBs
0100 0000 1111 1111	FREQ0 REG write (D15, D14 = 01), 14 MSBs = 00FF

Writing to a Phase Register

When writing to a phase register, Bit D15 and Bit D14 are set to 11. Bit D13 identifies which phase register is being loaded.

Table 12. Phase Register Bits

D15	D14	D13	D12	D11	D0
1	1	0	X	MSB 12 PHASE0 bits	LSB
1	1	1	X	MSB 12 PHASE1 bits	LSB

RESET FUNCTION

The reset function resets appropriate internal registers to 0 to provide an analog output of midscale. Reset does not reset the phase, frequency, or control registers. When the AD9833 is powered up, the part should be reset. To reset the AD9833, set the reset bit to 1. To take the part out of reset, set the bit to 0. A signal will appear at the DAC to output eight MCLK cycles after reset is set to 0.

Table 13. Applying Reset

Reset Bit	Result
0	No reset applied
1	Internal registers reset

SLEEP FUNCTION

Sections of the AD9833 that are not in use can be powered down to minimize power consumption. This is done using the SLEEP function. The parts of the chip that can be powered down are the internal clock and the DAC. The bits required for the SLEEP function are outlined in Table 14.

Table 14. Applying the SLEEP Function

SLEEP1 Bit	SLEEP12 Bit	Result
0	0	No power-down
0	1	DAC powered down
1	0	Internal clock disabled
1	1	Both the DAC powered down and the internal clock disabled

DAC Powered Down

This is useful when the AD9833 is used to output the MSB of the DAC data only. In this case, the DAC is not required; therefore, it can be powered down to reduce power consumption.

Internal Clock Disabled

When the internal clock of the AD9833 is disabled, the DAC output will remain at its present value because the NCO is no longer accumulating. New frequency, phase, and control words can be written to the part when the SLEEP1 control bit is active. The synchronizing clock is still active, which means that the selected frequency and phase registers can also be changed using the control bits. Setting the SLEEP1 bit to 0 enables the MCLK. Any changes made to the registers while SLEEP1 is active will be seen at the output after a certain latency.

VOUT PIN

The AD9833 offers a variety of outputs from the chip, all of which are available from the VOUT pin. The choice of outputs is the MSB of the DAC data, a sinusoidal output, or a triangle output.

The OPBITEN (D5) and mode (D1) bits in the control register are used to decide which output is available from the AD9833.

MSB of the DAC Data

The MSB of the DAC data can be output from the AD9833. By setting the OPBITEN (D5) control bit to 1, the MSB of the DAC data is available at the VOUT pin. This is useful as a coarse clock source. This square wave can also be divided by two before being output. The DIV2 (D3) bit in the control register controls the frequency of this output from the VOUT pin.

Sinusoidal Output

The SIN ROM is used to convert the phase information from the frequency and phase registers into amplitude information that results in a sinusoidal signal at the output. To have a sinusoidal output from the VOUT pin, set the mode (D1) bit to 0 and the OPBITEN (D5) bit to 0.

Triangle Output

The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC will produce a 10-bit linear triangular function. To have a triangle output from the VOUT pin, set the mode (D1) bit = 1.

Note that the SLEEP12 bit must be 0 (that is, the DAC is enabled) when using this pin.

Table 15. Various Outputs from VOUT

OPBITEN Bit	Mode Bit	DIV2 Bit	VOUT Pin
0	0	X[1]	Sinusoid
0	1	X[1]	Triangle
1	0	0	DAC data MSB/2
1	0	1	DAC data MSB
1	1	X[1]	Reserved

[1] X = don't care.

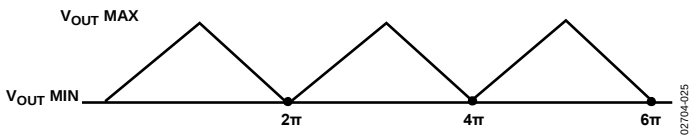

Figure 25. Triangle Output

APPLICATIONS INFORMATION

Because of the various output options available from the part, the AD9833 can be configured to suit a wide variety of applications.

One of the areas where the AD9833 is suitable is in modulation applications. The part can be used to perform simple modulation, such as FSK. More complex modulation schemes, such as GMSK and QPSK, can also be implemented using the AD9833.

In an FSK application, the two frequency registers of the AD9833 are loaded with different values. One frequency represents the space frequency, while the other represents the mark frequency. Using the FSELECT bit in the control register of the AD9833, the user can modulate the carrier frequency between the two values.

The AD9833 has two phase registers, which enables the part to perform PSK. With phase-shift keying, the carrier frequency is phase shifted, the phase being altered by an amount that is related to the bit stream being input to the modulator.

The AD9833 is also suitable for signal generator applications. Because the MSB of the DAC data is available at the VOUT pin, the device can be used to generate a square wave.

With its low current consumption, the part is suitable for applications in which it can be used as a local oscillator.

GROUNDING AND LAYOUT

The printed circuit board (PCB) that houses the AD9833 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in one place only. If the AD9833 is the only device requiring an AGND-to-DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD9833. If the AD9833 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9833.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD9833 to avoid noise coupling. The power supply lines to the AD9833 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the other side.

Good decoupling is important. The AD9833 should have supply bypassing of 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device.

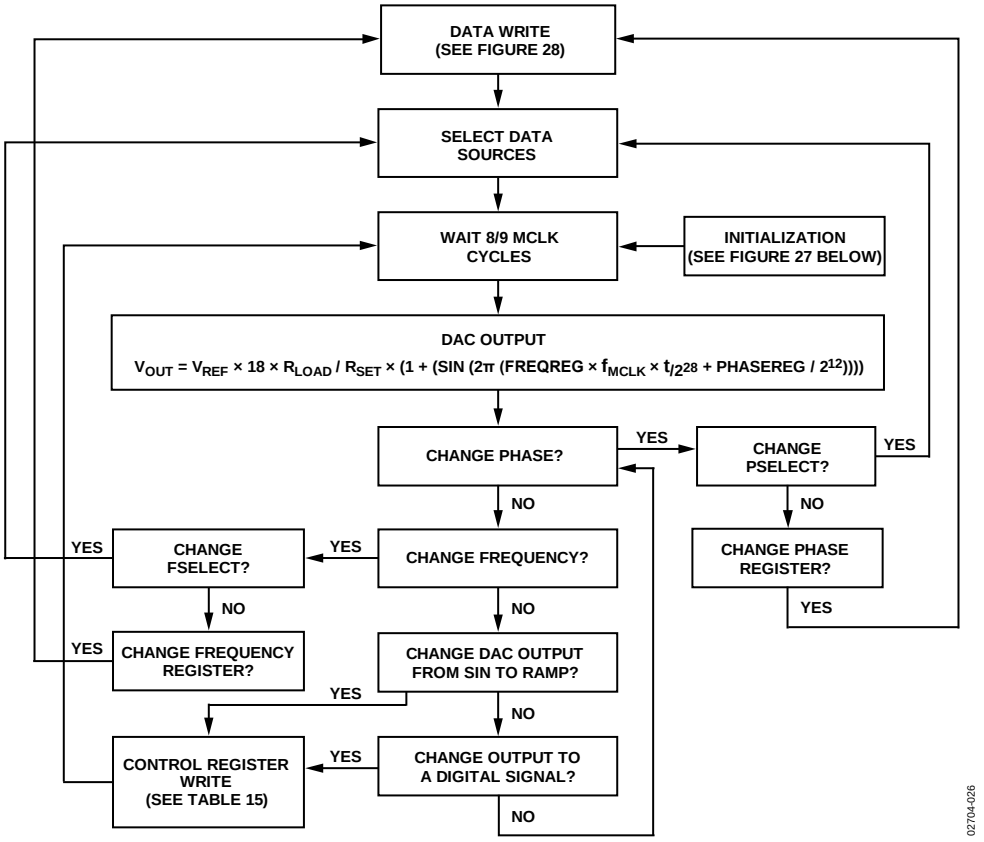

Figure 26. Flow Chart for AD9833 Initialization and Operation

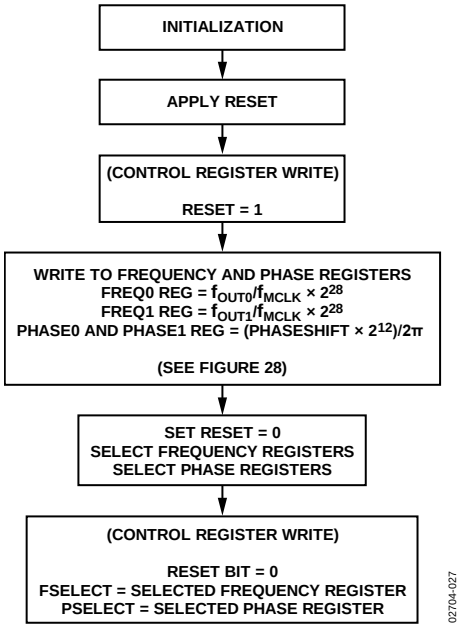

Figure 27. Initialization

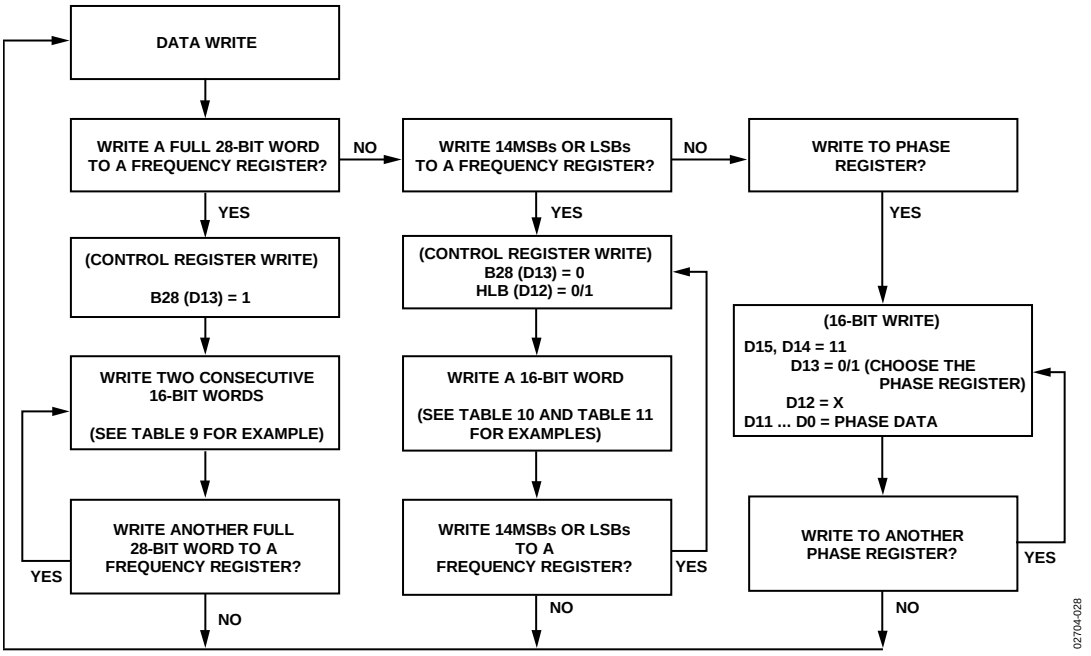

Figure 28. Data Writes